PRELIMINARY

NLT Technologies, Ltd.

TFT MONOCHROME LCD MODULE

For Topro Display Technology Co.,Ltd.

NL204153AM21-24A

54cm (21.3 Type)
QXGA
LVDS interface (4ports)

PRELIMINARY SPECIFICATION

DOD-PP-1563 (1st editon)

Signature of writer

Approved by K. Fujimoto	*Date*
K. FUJIMOTO	Feb. 1, 2013
Checked by	*Date*
Prepared by E. Yoshimura	*Date*
E. YOSHIMURA	Feb. 1, 2012

Published by

Product Planning Department
Sales Division
NLT Technologies, Ltd.

INTRODUCTION

• WARRANTY

NLT Technologies, Ltd. (hereinafter called "NLT") warrants that this product meets the product specifications set forth in this document. If this product under normal operation is found to be non-conforming to the product specifications, and such non-conformance is promptly notified to NLT within one (1) year after the delivery date, and further such non-conformance is solely attributable to NLT, NLT shall repair the non-conforming product or replace it with a conforming one, free of charge. However, this warranty does not apply to any non-conformance resulting from any one of the following:

1) Unauthorized or improper repair, maintenance or modification
2) Operation or use against specifications, instructions or warnings given by NLT
3) Any other causes attributable to customer

In case NLT repairs or replaces a product after the one (1) year warranty period, NLT shall be entitled to charge for such repair or replacement. Those replaced parts shall be covered with six (6)-month warranty period from the replacement day. Non-conforming products may be replaced with substitutes instead of repair when the manufacture of this product has been terminated.

EXCEPT AS EXPRESSLY SET FORTH HEREIN, NLT DISCLAIMS ANY WARRANTIES, EXPRESS OR IMPLIED, INCLUDING BUT NOT LIMITED TO MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE, AND DISCLAIMS ANY REMEDIES.

• MAINTENANCE

The specifications of maintenance parts are subject to change with equivalent or better quality. NLT will not accept maintenance for only mounting parts on circuit board (e.g. connector, fuse, capacitor, resistor, etc.) or only parts for backlight (e.g. reflector sheet, light guide plate, etc.). but for a whole module by unit.

If NLT plans to discontinue this product, NLT shall inform it to customers in six (6)-month advance from the issued date of official announcement. In addition, after the product discontinuation, NLT may replace a product with a whole product not repairing parts.

• CHANGE CONTROL

For the purpose of product improvement, this product design is subject to change for improvement in specifications, appearance, parts, circuits and so on. In case that the design change affects the product specifications, NLT shall inform it to customers in advance.

• HANDLING OF DOUBTFUL POINTS

Any question arising out of, or in connection with, this SPECIFICATION or any matter not stipulated herein will be settled each time upon consultation between both parties.

PRELIMINARY

CONTENTS

CONTENTS

1. OUTLINE

1.1 STRUCTURE AND PRINCIPLE

Monochrome LCD module NL204153AM21-24A is composed of the amorphous silicon thin film transistor liquid crystal display (a-Si TFT LCD) panel structure with driver LSIs for driving the TFT (Thin Film Transistor) array and a backlight.

The a-Si TFT LCD panel structure is injected liquid crystal material into a narrow gap between the TFT array glass substrate and a monochrome-filter glass substrate.

Grayscale data signals from a host system (e.g. signal generator, etc.) are modulated into best form for active matrix system by a signal processing board, and sent to the driver LSIs which drive the individual TFT arrays.

The TFT array as an electro-optical switch regulates the amount of transmitted light from the backlight assembly, when it is controlled by data signals. Monochrome images are created by regulating the amount of transmitted light through the TFT array.

1.2 APPLICATION

- Monochrome monitor system

1.3 FEATURES

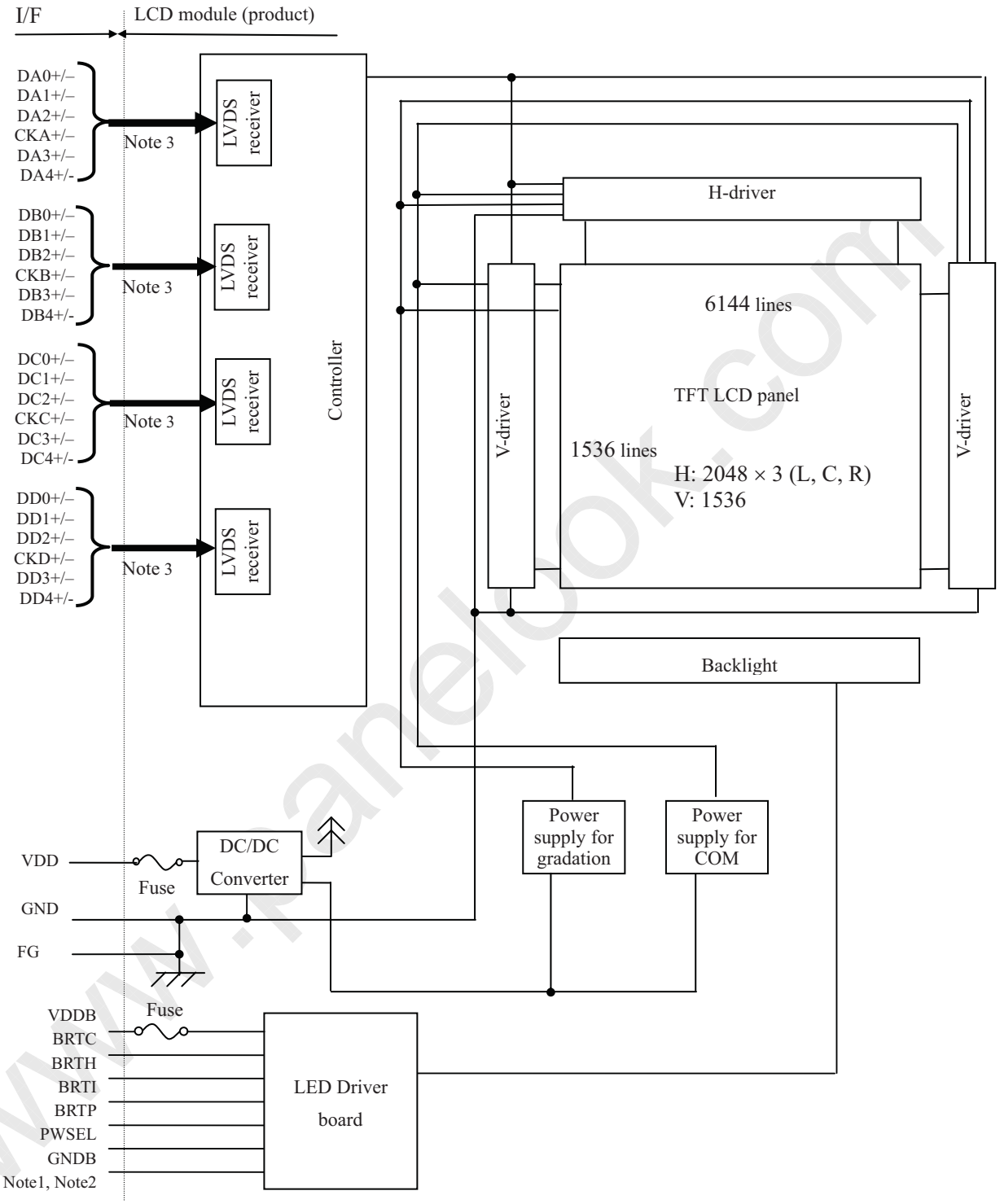
- Ultra-wide viewing angle (Super Fine TFT (SFT))
- High luminance
- High contrast
- Low reflection
- 1,024 gray scales per 1 sub-pixel (10-bit)
- LVDS interface
- Small foot print
- LED backlight type
- LED driver circuit Built-in

2. GENERAL SPECIFICATIONS

Display area	433.152 (H) × 324.864 (V) mm
Diagonal size of display	54cm (21.3 inches)
Drive system	a-Si TFT active matrix
Display grayscale	1,024 gray scales per 1 sub-pixel (10-bit) (3,072 gray scales per 1 pixel)
Pixel	2,048 (H) × 1,536 (V) pixels (1 pixel consists of 3 sub-pixels (LCR).)
Pixel arrangement	LCR vertical stripe
Sub-pixel pitch	0.0705 (H) × 0.2115 (V) mm
Pixel pitch	0.2115 (H) × 0.2115 (V) mm
Module size	457.0 (W) × 350.0 (H) × 21.5 (D) mm (typ.)
Weight	2,700 g (typ.)
Contrast ratio	1,400:1 (typ.)
Viewing angle	*At the contrast ratio ≥ 10:1* • Horizontal: Right side 88° (typ.), Left side 88° (typ.) • Vertical: Up side 88° (typ.), Down side 88° (typ.)
Designed viewing direction	Viewing angle with optimum grayscale (γ≒ DICOM): Normal axis (perpendicular) Note1
Polarizer surface	Antiglare
Polarizer pencil-hardness	2H (min.) [by JIS K5600]
Response time	*Ton+Toff (10%←→90%)* 40ms (typ.)
Luminance	*At the maximum luminance control* 1,700cd/m^2 (typ.)
Signal system	4 ports LVDS interface (Characteristics of AC receiver THC63LVD104S×2pcs, THine Electronics, Inc. or equivalent) [LCR 10-bit signals, Data enable signal (DE), Dot clock (CK)]
Power supply voltage	LCD panel signal processing board: 12.0V LED driver board: 12.0V
Backlight	LED backlight type built in LED Driver Circuit
Power consumption	*At checkered flag pattern, the maximum luminance control* 37.0W (typ.)

Note1: When the product luminance is 450cd/m^2, the gamma characteristic is designed to γ≒ DICOM.

3. BLOCK DIAGRAM



Note1: Relations between GND (Signal ground), FG (Frame ground) and GNDB (LED driver board ground) in the LCD module are as follows.

GND - FG	Connected
GND - GNDB	Not connected
FG - GNDB	Not connected

Note2 GND, FG and GNDB must be connected to customer equipment's ground, and it is recommended that these grounds be connected together in customer equipment.

Note3 Each pair of the LVDS signal has a 100Ω terminating resistance between D+ and D-.

4. DETAILED SPECIFICATIONS

4.1 MECHANICAL SPECIFICATIONS

Parameter	Specification	Unit
Module size	457.0 ±0.5 (W) × 350.0 ±0.5 (H) × 21.5 (typ., D) 23.0 (max., D) Note1, Note2	mm
Display area	433.152 (H) × 324.864 (V) Note2	mm
Weight	2,700 (typ.), 2,980 (max.)	g

Note1: Excluding warpage of the cover for LED driver board.
Note2: See "**11. OUTLINE DRAWINGS**".

4.2 ABSOLUTE MAXIMUM RATINGS

Parameter			Symbol	Rating	Unit	Remarks
Power supply voltage	LCD panel signal processing board		VDD	-0.3 to +14.0	V	-
	LED driver board		VDDB	-0.3 to +15.0	V	
Input voltage for signals	LCD panel signal processing board Note1		Vi	-0.3 to +2.8	V	VDD= 12.0V
	LED driver board	BRTI signal	VBI	-0.3 to +1.5	V	VDDB= 12.0V
		BRTP signal	VBP	-0.3 to +5.5	V	
		BRTC signal	VBC	-0.3 to +5.5	V	
		PWSEL signal	VBS	-0.3 to +5.5	V	
Storage temperature			Tst	-20 to +60	°C	-
Operating temperature		Front surface	TopF	0 to +60	°C	Note2
		Rear surface	TopR	0 to + 60	°C	Note3
Relative humidity Note4			RH	≤ 95	%	Ta ≤ 40°C
				≤ 85	%	40°C < Ta ≤ 50°C
				≤ 70	%	50°C < Ta ≤ 55°C
Absolute humidity Note4			AH	≤ 73 Note5	g/m^3	Ta > 55°C
Operating altitude			-	≤ 5,100	m	0°C ≤ Ta ≤ 55°C
Storage altitude			-	≤ 13,600	m	-20°C ≤ Ta ≤ 60°C

Note1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-,BSEL.
Note2: Measured at LCD panel surface (including self-heat)
Note3: Measured at LCD module's rear shield surface (including self-heat)
Note4: No condensation
Note5: Water amount at Ta= 55°C and RH= 70%

4.3 ELECTRICAL CHARACTERISTICS

4.3.1 LCD panel signal processing board

(Ta= 25°C)

Parameter		Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage		VDD	10.8	12.0	13.2	V	-
Power supply current		IDD	-	590 Note1	980 Note2	mA	at VDD= 12.0V
Permissible ripple voltage		VRP	-	-	100	mVp-p	for VDD
Differential input threshold voltage	High	VTH	-	-	+100	mV	at VCM= 1.2V Note3, Note4
	Low	VTL	-100	-	-	mV	
Input voltage swing		VI	0	-	2.4	V	Note4
Terminating resistance		RT	-	100	-	Ω	-

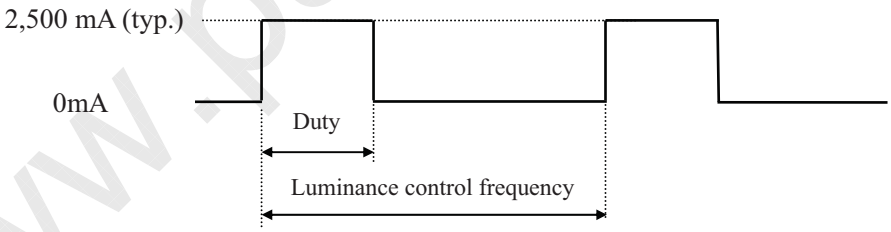
Note1: Checkered flag pattern (by EIAJ ED-2522)
Note2: Pattern for maximum current
Note3: Common mode voltage for LVDS driver
Note4: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-

4.3.2 LED Driver board

(Ta= 25°C)

Parameter			Symbol	min.	typ.	max.	Unit	Remarks
Power supply voltage			VDDB	11.4	12.0	12.6	V	-
Power supply current			IDDB	-	2,500	3,300	mA	VDDB= 12.0V, At the maximum luminance control
Input voltage for signals	BRTI signal		VBI	0	-	1.0	V	-
	BRTP signal	High	VBPH	2.0	-	5.25	V	
		Low	VBPL	0	-	0.8	V	
	BRTC signal	High	VBCH	2.0	-	5.25	V	
		Low	VBCL	0	-	0.8	V	
	PWSEL signal	High	VBSH	2.0	-	5.25	V	
		Low	VBSL	0	-	0.8	V	
Input current for signals	BRTI signal		IBI	-200	-	-100	µA	
	BRTP signal	High	IBPH	-	-	1,000	µA	
		Low	IBPL	-600	-	-	µA	
	BRTC signal	High	IBCH	-	-	300	µA	
		Low	IBCL	-300	-	-	µA	
	PWSEL signal	High	IPSH	-	-	1,000	µA	
		Low	IPSL	-600	-	-	µA	

4.3.3 LED Driver board current wave



Duty:At the maximum luminance control 100% to at the minimum luminance control 1%.
Luminance control frequency: 270Hz (typ.)

Note1: Luminance control frequency indicate the input pulse frequency, when select the external pulse control. See "**4.6.2 Detail of BRTP timing**".

Note2: The power supply lines (VDDB and GNDB) have large ripple voltage during luminance control.
There is the possibility that the ripple voltage produces acoustic noise and signal wave noise in audio circuit and so on. Put a capacitor (5,000 to 6,000µF) between the power supply lines (VDDB and GNDB) to reduce the noise, if the noise occurred in the circuit.

4.3.4 Power supply voltage ripple

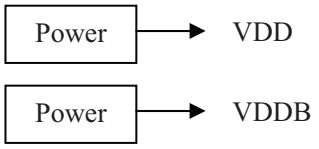
This product works, even if the ripple voltage levels are beyond the permissible values as following the table, but there might be noise on the display image.

Power supply voltage		Ripple voltage Note1 (Measure at input terminal of power supply)	Unit
VDD	12.0V	≤ 100	mVp-p
VDDB	12.0V	≤ 200	mVp-p

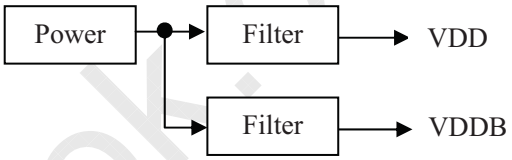
Note1: The permissible ripple voltage includes spike noise.
Note2: The load variation influence does not include.

Example of the power supply connection

a) Separate the power supply



b) Put in the filter



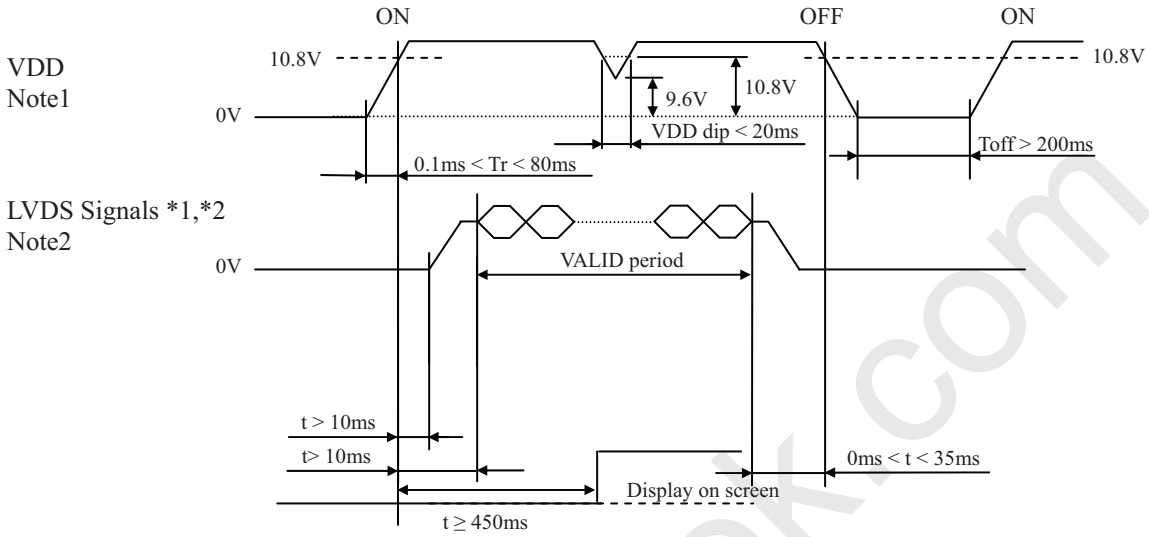
4.3.5 Fuse

Parameter	Fuse		Rating	Fusing current	Remarks
	Type	Supplier			
VDD	FCC16202AB	KAMAYA ELECTRIC Co., Ltd.	2.0 A 32 V	4.0A, 5 seconds maximum	Note1
VDDB	CCF1N10	KOA Corporation	10A 60V	20 A, 1 seconds maximum	
	TF16AT5.00T		5.0A 32V	10 A, 5 seconds maximum	

Note1: The power supply capacity should be more than the fusing current. If it is less than the fusing current, the fuse may not blow in a short time, and then nasty smell, smoke and so on may occur.

4.4 POWER SUPPLY VOLTAGE SEQUENCE

4.4.1 LCD panel signal processing board



*1: DA0+/-, DA1+/-, DA2+/-, DA3+/-, DA4+/-, CKA+/-, DB0+/-, DB1+/-, DB2+/-, DB3+/-, DB4+/-, CKB+/-, DC0+/-, DC1+/-, DC2+/-, DC3+/-, DC4+/-, CKC+/-, DD0+/-, DD1+/-, DD2+/-, DD3+/-, DD4+/-, CKD+/-

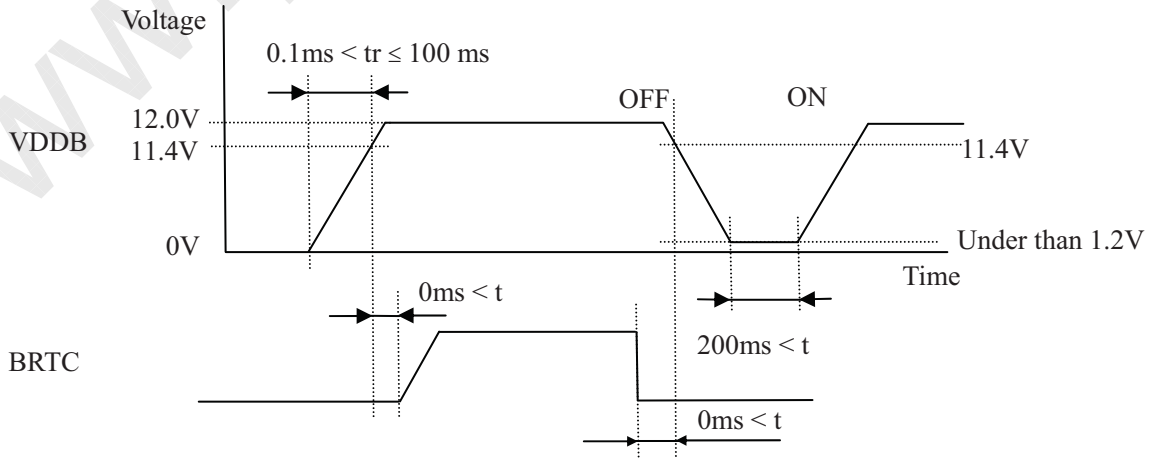
*2: LVDS signals should be measured at the terminal of 100 Ω resistance.

Note1: If there is a voltage variation (voltage drop) at the rising edge of VCC below 10.8V, there is a possibility that a product does not work due to a protection circuit.

Note2: LVDS signals must be set to Low or High-impedance, except the VALID period (See above sequence diagram), in order to avoid the circuitry damage.
If some of signals are cut while this product is working, even if the signal input to it once again, it might not work normally. If a customer stops the display and function signals, VDD also must be shut down.

Note3: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

4.4.2 LED driver board



Note1: The backlight should be turned on within the valid period of LVDS signals, in order to avoid unstable data display.

Note2: If tr is more than 100 ms, the backlight will be turned off by a protection circuit for LED driver board.

Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5 CONNECTIONS AND FUNCTIONS FOR INTERFACE PINS

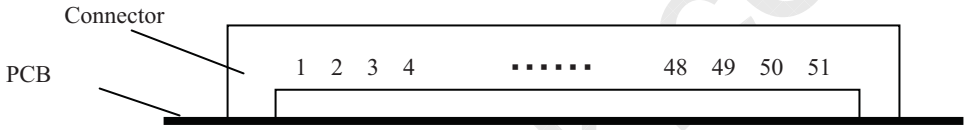
4.5.1 LCD panel signal processing board

CN1 socket (LCD module side): FI-RE51S-HF (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-RE51HL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	Note1
2	GND	Ground	
3	GND	Ground	
4	DA0-	Pixel data A0	LVDS differential data input Note2
5	DA0+		
6	GND	Ground	Note1
7	DA1-	Pixel data A1	LVDS differential data input Note2
8	DA1+		
9	GND	Ground	Note1
10	DA2-	Pixel data A2	LVDS differential data input Note2
11	DA2+		
12	GND	Ground	Note1
13	CKA-	Pixel clock A	LVDS differential data input Note2
14	CKA+		
15	GND	Ground	Note1
16	DA3-	Pixel data A3	LVDS differential data input Note2
17	DA3+		
18	GND	Ground	Note1
19	DA4-	Pixel data A4	LVDS differential data input Note2
20	DA4+		
21	GND	Ground	Note1
22	DB0-	Pixel data B0	LVDS differential data input Note2
23	DB0+		
24	GND	Ground	Note1
25	DB1-	Pixel data B1	LVDS differential data input Note2
26	DB1+		
27	GND	Ground	Note1
28	DB2-	Pixel data B2	LVDS differential data input Note2
29	DB2+		
30	GND	Ground	Note1
31	CKB-	Pixel clock B	LVDS differential data input Note2
32	CKB+		
33	GND	Ground	Note1
34	DB3-	Pixel data B3	LVDS differential data input Note2
35	DB3+		
36	GND	Ground	Note1
37	DB4-	Pixel data B4	LVDS differential data input Note2
38	DB4+		
39	GND	Ground	Note1

40	GND	Ground	Note1
41	RSEV	-	Keep this pin Open.
42	RSEV	-	Keep this pin Open.
43	RSEV	-	Keep this pin Open.
44	RSEV	-	Keep this pin Open.
45	GND	Ground	Note1
46	GND	Ground	Note1
47	GND	Ground	Note1
48	RSEV	-	Keep this pin Open.
49	RSEV	-	Keep this pin Open.
50	RSEV	-	Keep this pin Open.
51	GND	Ground	Note1

CN1: Insert surface side



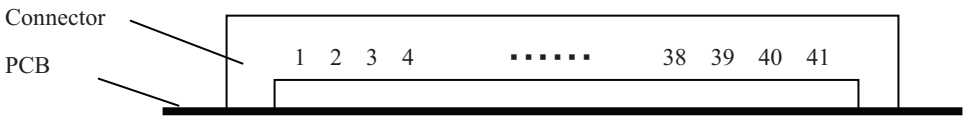
Note1: All GND terminals should be used without any non-connected lines.

Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

CN2 socket (LCD module side): FI-RE41S-HF (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: FI-RE41HL (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Signal	Remarks
1	GND	Ground	
2	GND	Ground	Note1
3	GND	Ground	
4	DC0-	Pixel data C0	LVDS differential data input Note2
5	DC0+		
6	GND	Ground	Note1
7	DC1-	Pixel data C1	LVDS differential data input Note2
8	DC1+		
9	GND	Ground	Note1
10	DC2-	Pixel data C2	LVDS differential data input Note2
11	DC2+		
12	GND	Ground	Note1
13	CKC-	Pixel clock C	LVDS differential data input Note2
14	CKC+		
15	GND	Ground	Note1
16	DC3-	Pixel data C3	LVDS differential data input Note2
17	DC3+		
18	GND	Ground	Note1
19	DC4-	Pixel data C4	LVDS differential data input Note2
20	DC4+		
21	GND	Ground	Note1
22	DD0-	Pixel data D0	LVDS differential data input Note2
23	DD0+		
24	GND	Ground	Note1
25	DD1-	Pixel data D1	LVDS differential data input Note2
26	DD1+		
27	GND	Ground	Note1
28	DD2-	Pixel data D2	LVDS differential data input Note2
29	DD2+		
30	GND	Ground	Note1
31	CKD-	Pixel clock D	LVDS differential data input Note2
32	CKD+		
33	GND	Ground	Note1
34	DD3-	Pixel data D3	LVDS differential data input Note2
35	DD3+		
36	GND	Ground	Note1
37	DD4-	Pixel data D4	LVDS differential data input Note2
38	DD4+		
39	GND	Ground	Note1
40	GND	Ground	Note1
41	GND	Ground	Note1

CN2: Insert surface side

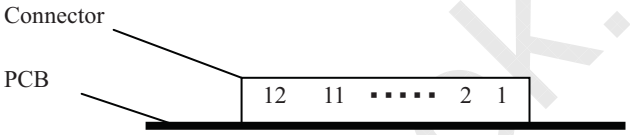


Note1: All GND terminals should be used without any non-connected lines.
Note2: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

CN3 socket (LCD module side): IL-Z-12PL-SMTYE (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: IL-Z-12S S125C (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	VDD	Power supply	Note1
2	VDD		
3	VDD		
4	VDD		
5	VDD		
6	VDD		
7	GND	Signal ground	Note1
8	GND		
9	GND		
10	GND		
11	GND		
12	GND		

CN3: Insert surface side



Note1: All VDD and GND terminals should be used without any non-connected lines.

4.5.2 LED driver board

CN201 socket (LCD module side): DF3Z-10P-2H (2*) (HIROSE ELECTRIC Co,.Ltd.)
Adaptable plug: DF3-10S-2C (HIROSE ELECTRIC Co,.Ltd.)

Pin No.	Symbol	Function	Description
1	GNDB	LED driver board ground	Note1
2	GNDB		
3	GNDB		
4	GNDB		
5	GNDB		
6	VDDB	Power supply	Note1
7	VDDB		
8	VDDB		
9	VDDB		
10	VDDB		

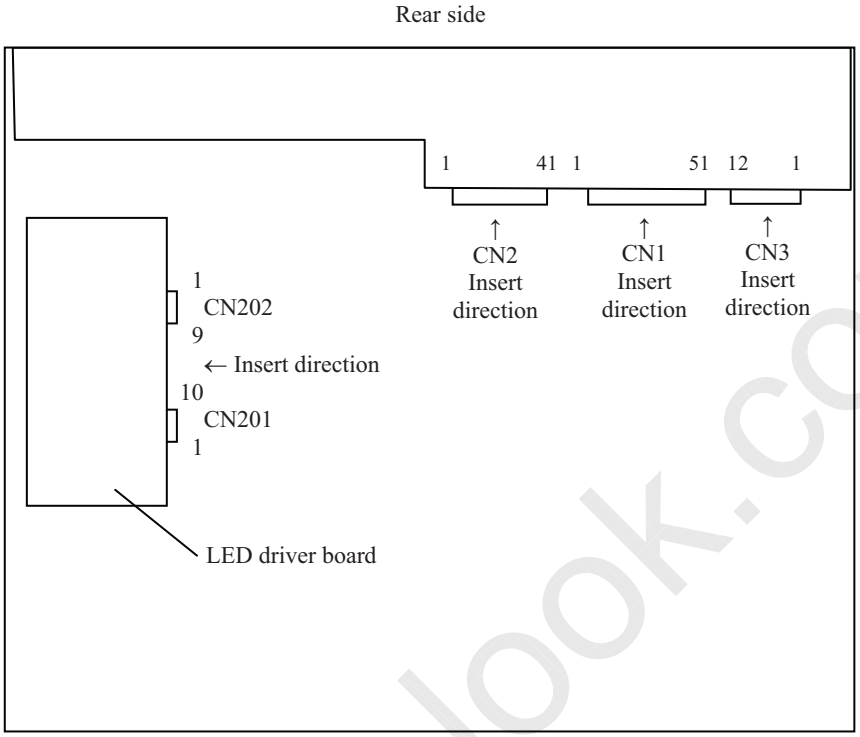
Note1: All VDDB and GNDB terminals should be used without any non-connected lines.

CN202 socket (LCD module side): IL-Z-9PL-SMTYE (Japan Aviation Electronics Industry Limited (JAE))
Adaptable plug: IL-Z-9S-S125C3 (Japan Aviation Electronics Industry Limited (JAE))

Pin No.	Symbol	Function	Description
1	GNDB	LED driver board ground	Note1
2	GNDB		
3	N.C.	-	Keep this pin Open.
4	BRTC	Backlight ON/OFF control signal	High or Open: Backlight ON Low Backlight OFF
5	BRTH	Luminance control terminal	Note2
6	BRTI		
7	BRTP	BRTP signal	
8	GNDB	LED driver board ground	Note1
9	PWSEL	Selection of luminance control signal method	Note2, Note3

Note1: All GNDB terminals should be used without any non-connected lines.
Note2: See "**4.6 LUMINANCE CONTROL** ".
Note3: When VDDB is 0V or BRTC is Low, PWSEL must be set to Low or Open.

4.5.3 Positions of socket

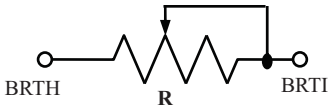


4.6 LUMINANCE CONTROL

4.6.1 Luminance control methods

<table>
<tr><th>Method</th><th>Adjustment and luminance ratio</th><th>PWSEL terminal</th><th>BRTP terminal</th></tr>
<tr><td>Variable resistor control

Note1</td><td>• Adjustment

The variable resistor (R) for luminance control should be 10kΩ ±5%, 1/10W. Minimum point of the resistance is the minimum luminance and maximum point of the resistance is the maximum luminance.
The resistor (R) must be connected between BRTH-BRTI terminals.
 

• Luminance ratio Note3
<table><tr><th>Resistance</th><th>Luminance ratio</th></tr><tr><td>0 kΩ</td><td>0% (Min. Luminance)</td></tr><tr><td>10 kΩ</td><td>100% (Max. Luminance)</td></tr></table></td><td rowspan="2">High or Open</td><td rowspan="2">Open</td></tr>
<tr><td>Voltage control

Note1</td><td>• Adjustment

Voltage control method works, when BRTH terminal is 0V and VBI voltage is input between BRTI-BRTH terminals. This control method can carry out continuation adjustment of luminance.
Luminance is the maximum when BRTI terminal is Open

• Luminance ratio Note3
<table><tr><th>BRTI Voltage (VBI)</th><th>Luminance ratio</th></tr><tr><td>0 V</td><td>0% (Min. Luminance)</td></tr><tr><td>1.0 V</td><td>100% (Max. Luminance)</td></tr></table></td></tr>
<tr><td>Pulse width modulation

Note1
Note2
Note4</td><td>• Adjustment

Pulse width modulation (PWM) method works, when PWSEL terminal is Low and PWM signal (BRTP signal) is input into BRTP terminal. The luminance is controlled by duty ratio of BRTP signal.

• Luminance ratio Note3
<table><tr><th>Duty ratio</th><th>Luminance ratio</th></tr><tr><td>0.01</td><td>1% (Min. Luminance)
(At frequency: 325 Hz)</td></tr><tr><td>1.0</td><td>100% (Max. Luminance)</td></tr></table></td><td>Low</td><td>BRTP signal</td></tr>
</table>

Note1: In case of the variable resistor control method and the voltage control method, noises may appear on the display image depending on the input signals timing for LCD panel signal processing board.
Use PWM method, if interference noises appear on the display image!

Note2: The LED driver board will stop working, if the Low period of BRTP signal is more than 50ms while BRTC signal is High or Open. Then the backlight will not turn on anymore, even if BRTP signal is input again. This is not out of order. The LED driver board will start to work when power is supplied again.

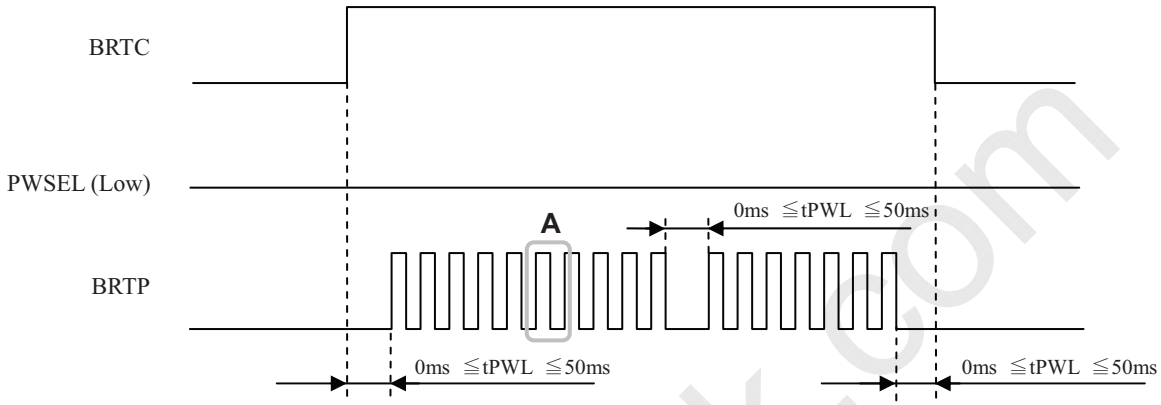
Note3: These data are the target values.

Note4: See "**4.6.2 Detail of BRTP timing**".

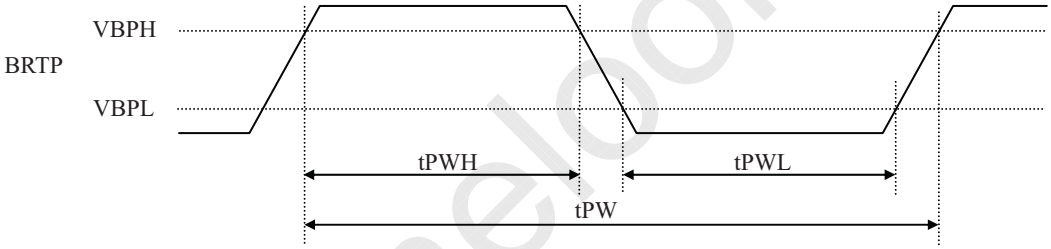
4.6.2 Detail of BRTP timing

(1) Timing diagrams

• Outline chart



• Detail of **A** part



(2) Each parameter

Parameter	Symbol	min.	typ.	max.	Unit	Remarks
PWM frequency	f_{PWM}	185	-	1,000	Hz	Note1,2,3
PWM duty ratio	DR_{PWM}	1	-	100	%	Note4,5
PWM pulse width	tPWH	30	-	-	µs	Note1,4,5

Note1: Definition of parameters is as follows.

$$f_{PWM} = \frac{1}{tPW}, \quad DL = \frac{tPWH}{tPW}$$

Note2: A recommended f_{PWM} value is as follows.

$$f_{PWM} = \frac{2n-1}{4} \times fv$$

(n= integer, fv= frame frequency of LCD module)

Note3: Depending on the frequency used, so noise may appear on the screen, please conduct a thorough evaluation.

Note4: While the BRTC signal is high, do not set the tPWH (PWM pulse width) is less than 30µs. It may cause abnormal working of the backlight. In this case, turn the backlight off and then on again by BRTC signal.

Note5: Regardless of the PWM frequency, both PWM duty ratio and PWM pulse width must be always more than the minimum values.

4.7 METHOD OF CONNECTION FOR LVDS TRANSMITTER

	Bit mapping	Transmitter Pin Assign: Single type LVDS Tx	Transmitter Pin Assign: Dual type LVDS Tx (Thine THC63LVD1023B)	Output Connector		CN1: Pin No.	CN1: Signal Name
odd Pixel data A	LA4	TA0	R14			-	-
	LA5	TA1	R15	ATA-	→	4	DA0-
	LA6	TA2	R16				
	LA7	TA3	R17	ATA+	→	5	DA0+
	LA8	TA4	R18				
	LA9	TA5	R19				
	CA4	TA6	G14			-	-
	CA5	TB0	G15				
	CA6	TB1	G16	ATB-	→	7	DA1-
	CA7	TB2	G17				
	CA8	TB3	G18	ATB+	→	8	DA1+
	CA9	TB4	G19				
	RA4	TB5	B14				
	RA5	TB6	B15			-	-
	RA6	TC0	B16				
	RA7	TC1	B17	ATC-	→	10	DA2-
	RA8	TC2	B18				
	RA9	TC3	B19	ATC+	→	11	DA2+
	Hsync	TC4	Hsync				
	Vsync	TC5	Vsync				
	DE	TC6	DE			-	-
	LA2	TD0	R12				
	LA3	TD1	R13	ATD-	→	16	DA3-
	CA2	TD2	G12				
	CA3	TD3	G13	ATD+	→	17	DA3+
	RA2	TD4	B12				
	RA3	TD5	B13				
	N.C.	TD6	-			-	-
	LA0	TE0	R10				
	LA1	TE1	R11			19	DA4-
	CA0	TE2	G10	ATE-	→		
	CA1	TE3	G11			20	DA4+
	RA0	TE4	B10	ATE+	→		
	RA1	TE5	B11				
	N.C.	TE6	-			-	-
	CLK	CLK	CLK	ATCLK-	→	13	CKA-
				ATCLK+	→	14	CKA+
even Pixel data B	LB4	TA0	R14			-	-
	LB5	TA1	R15	BTA-	→	22	DB0-
	LB6	TA2	R16				
	LB7	TA3	R17	BTA+	→	23	DB0+
	LB8	TA4	R18				
	LB9	TA5	R19				
	CB4	TA6	G14			-	-
	CB5	TB0	G15				
	CB6	TB1	G16	BTB-	→	25	DB1-
	CB7	TB2	G17				
	CB8	TB3	G18	BTB+	→	26	DB1+
	CB9	TB4	G19				
	RB4	TB5	B14				
	RB5	TB6	B15			-	-
	RB6	TC0	B16				
	RB7	TC1	B17	BTC-	→	28	DB2-
	RB8	TC2	B18				
	RB9	TC3	B19	BTC+	→	29	DB2+
	Hsync	TC4	Hsync				
	Vsync	TC5	Vsync				
	DE	TC6	DE			-	-
	LB2	TD0	R12				
	LB3	TD1	R13	BTD-	→	34	DB3-
	CB2	TD2	G12				
	CB3	TD3	G13	BTD+	→	35	DB3+
	RB2	TD4	B12				
	RB3	TD5	B13				
	N.C.	TD6	-			-	-
	LB0	TE0	R10				
	LB1	TE1	R11			37	DB4-
	CB0	TE2	G10	BTE-	→		
	CB1	TE3	G11			38	DB4+
	RB0	TE4	B10	BTE+	→		
	RB1	TE5	B11				
	N.C.	TE6	-			-	-
	CLK	CLK	CLK	BTCLK-	→	31	CKB-
				BTCLK+	→	32	CKB+

	Bit mapping	Transmitter Pin Assign: Single type LVDS Tx	Transmitter Pin Assign: Dual type LVDS Tx (Thine THC63LVD1023B)	Output Connector		CN2 Pin No.	CN2 Signal Name
odd Pixel data C	LC4	TA0	R14			-	-
	LC5	TA1	R15	CTA-	→	4	DC0-
	LC6	TA2	R16				
	LC7	TA3	R17	CTA+	→	5	DC0+
	LC8	TA4	R18				
	LC9	TA5	R19				
	CC4	TA6	G14			-	-
	CC5	TB0	G15				
	CC6	TB1	G16	CTB-	→	7	DC1-
	CC7	TB2	G17				
	CC8	TB3	G18	CTB+	→	8	DC1+
	CC9	TB4	G19				
	RC4	TB5	B14				
	RC5	TB6	B15			-	-
	RC6	TC0	B16				
	RC7	TC1	B17	CTC-	→	10	DC2-
	RC8	TC2	B18				
	RC9	TC3	B19	CTC+	→	11	DC2+
	Hsync	TC4	Hsync				
	Vsync	TC5	Vsync				
	DE	TC6	DE			-	-
	LC2	TD0	R12				
	LC3	TD1	R13	CTD-	→	16	DC3-
	CC2	TD2	G12				
	CC3	TD3	G13	CTD+	→	17	DC3+
	RC2	TD4	B12				
	RC3	TD5	B13				
	N.C.	TD6	-			-	-
	LC0	TE0	R10				
	LC1	TE1	R11	CTE-	→	19	DC4-
	CC0	TE2	G10				
	CC1	TE3	G11	CTE+	→	20	DC4+
	RC0	TE4	B10				
	RC1	TE5	B11				
	N.C.	TE6	-			-	-
	CLK	CLK	CLK	CTCLK-	→	13	CKC-
				CTCLK+	→	14	CKC+
even Pixel data D	LD4	TA0	R14			-	-
	LD5	TA1	R15	DTA-	→		
	LD6	TA2	R16				
	LD7	TA3	R17	DTA+	→	23	DD0+
	LD8	TA4	R18				
	LD9	TA5	R19				
	CD4	TA6	G14			-	-
	CD5	TB0	G15				
	CD6	TB1	G16	DTB-	→	25	DD1-
	CD7	TB2	G17				
	CD8	TB3	G18	DTB+	→	26	DD1+
	CD9	TB4	G19				
	RD4	TB5	B14				
	RD5	TB6	B15			-	-
	RD6	TC0	B16				
	RD7	TC1	B17	DTC-	→	28	DD2-
	RD8	TC2	B18				
	RD9	TC3	B19	DTC+	→	29	DD2+
	Hsync	TC4	Hsync				
	Vsync	TC5	Vsync				
	DE	TC6	DE			-	-
	LD2	TD0	R12				
	LD3	TD1	R13	DTD-	→	34	DD3-
	CD2	TD2	G12				
	CD3	TD3	G13	DTD+	→	35	DD3+
	RD2	TD4	B12				
	RD3	TD5	B13				
	N.C.	TD6	-			-	-
	LD0	TE0	R10				
	LD1	TE1	R11	DTE-	→	37	DD4-
	CD0	TE2	G10				
	CD1	TE3	G11	DTE+	→	38	DD4+
	RD0	TE4	B10				
	RD1	TE5	B11				
	N.C.	TE6	-			-	-
	CLK	CLK	CLK	DTCLK-	→	31	CKD-
				DTCLK+	→	32	CKD+

Note1: Twist pair wires with 100Ω (Characteristic impedance) should be used between LCD panel signal processing board and LVDS transmitter.

PRELIMINARY

NLT Technologies Confidential and Proprietary

4.8 DISPLAY GRAYSCALE AND INPUT DATA SIGNALS

This product can display 1,024 gray scales in each LCR sub-pixel and 3,072 gray scales per 1 pixel. Also the relation between display gray scale and input data signals is as follows.

Display gray scale		Data signal (0: Low level, 1: High level)																													
		LA9	LA8	LA7	LA6	LA5	LA4	LA3	LA2	LA1	LA0	CA9	CA8	CA7	CA6	CA5	CA4	CA3	CA2	CA1	CA0	RA9	RA8	RA7	RA6	RA5	RA4	RA3	RA2	RA1	RA0
		LB9	LB8	LB7	LB6	LB5	LB4	LB3	LB2	LB1	LB0	CB9	CB8	CB7	CB6	CB5	CB4	CB3	CB2	CB1	CB0	RB9	RB8	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0
		LC9	LC8	LC7	LC6	LC5	LC4	LC3	LC2	LC1	LC0	CC9	CC8	CC7	CC6	CC5	CC4	CC3	CC2	CC1	CC0	RD9	RC8	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0
		LD9	LD8	LD7	LD6	LD5	LD4	LD3	LD2	LD1	LD0	CD9	CD8	CD7	CD6	CD5	CD4	CD3	CD2	CD1	CD0	RD9	RD8	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
Left sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	↑						:										:										:				
	↓						:										:										:				
	bright	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Center sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
	↑						:										:										:				
	↓						:										:										:				
	bright	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0
	White	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
Right sub-pixel gray scale	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
	dark	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
	↑						:										:										:				
	↓						:										:										:				
	bright	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	1
		0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	0
	White	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1

4.9 INPUT SIGNAL TIMINGS

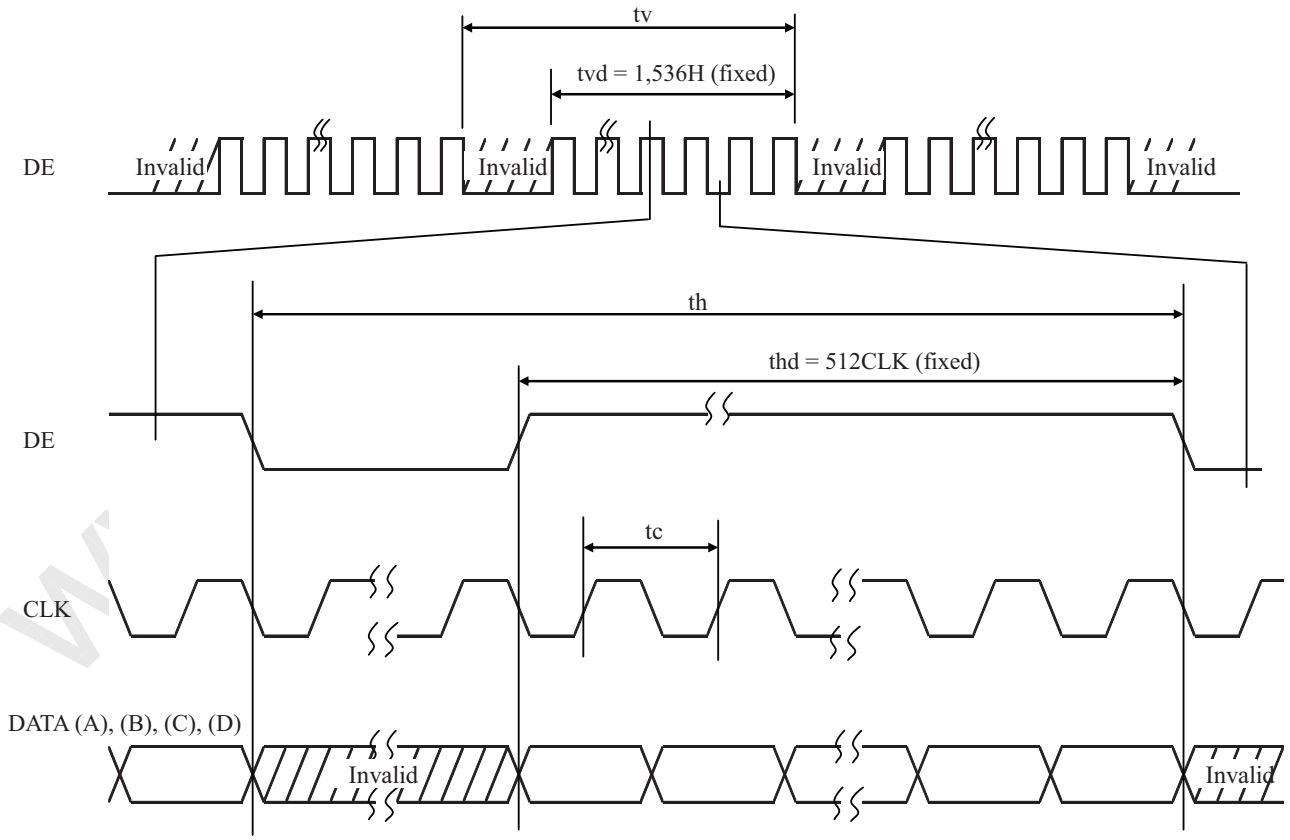
4.9.1 Timing characteristics

fv=60Hz

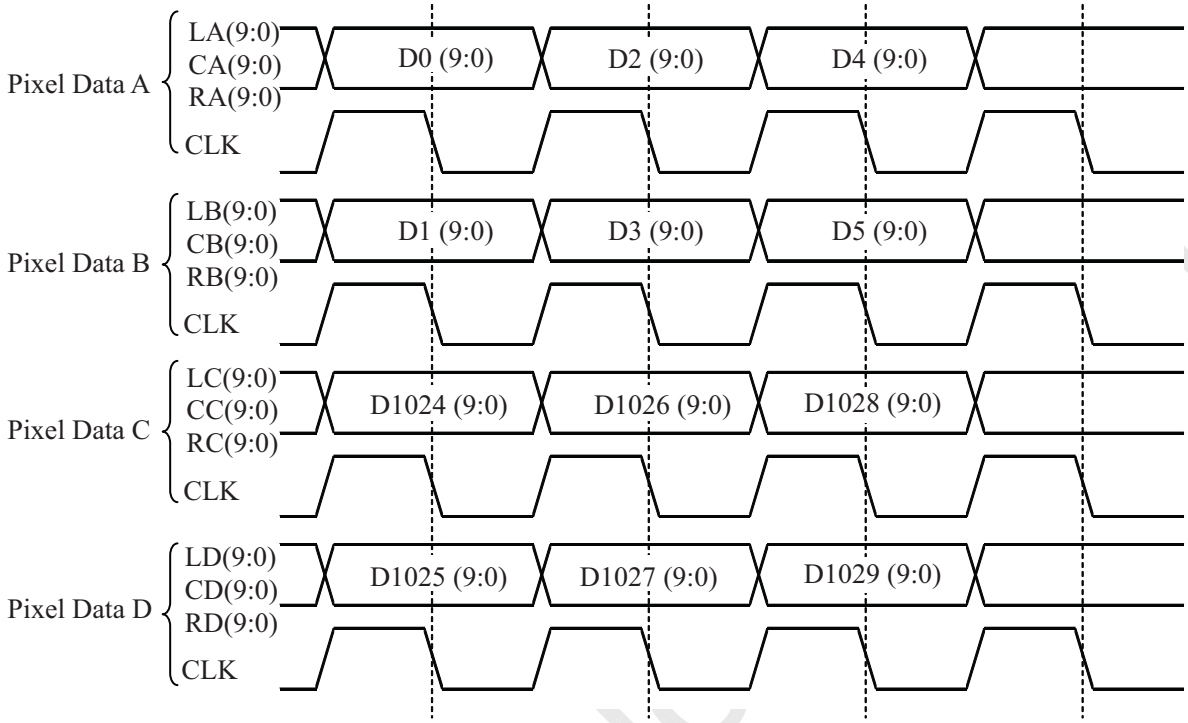
Parameter			Symbol	min.	typ.	max.	Unit	Remarks
CLK	Frequency		1/ tc	60.0	65.0	66.0	MHz	-
	Duty		-	See the data sheet of LVDS transmitter.			-	-
	Rise time, Fall time		-				ns	-
DE	Horizontal	Cycle	th	10.34	10.34	10.77	µs	96,72kHz(typ.) Note1
				640	672	700	CLK	
		Display period	thd	512			CLK	-
	Vertical	Cycle	tv	15.47	16.667	17.9	ms	60.0Hz(typ.)
				1547	1612	1628	H	
		Display period	tvd	1536			H	-
	CLK-DE	Setup time	-	See the data sheet of LVDS transmitter.			ns	-
		Hold time	-				ns	-
	Rise time, Fall time		-				ns	-

Note1: During operation, fluctuation of horizontal cycle should be within ±1 CLK.

4.9.2 Input signal timing chart

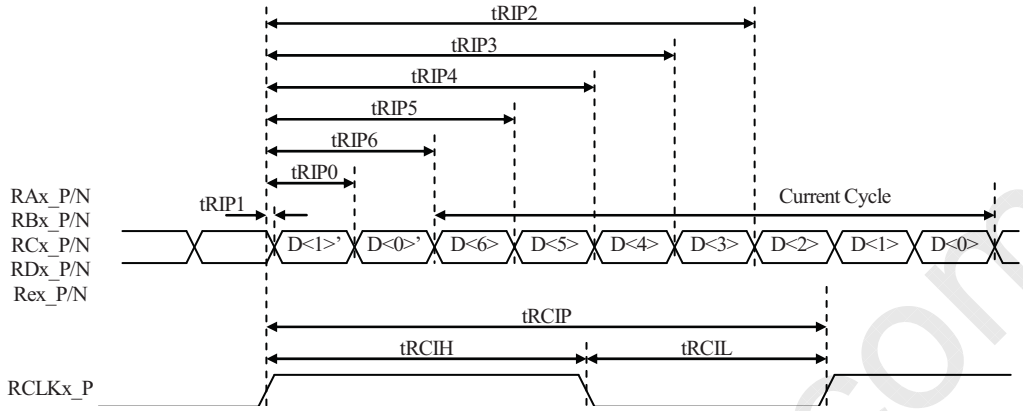


4.10 LVDS DATA TARANSMISSION METHOD



4.11 LVDS Rx AC SPEC

Symbol	Parameter	min.	typ.	max.	Units
t_{RCIP}	RCLKx_P Period	11.76	-	40.0	ns
t_{RCIH}	RCLKx_P High pulse width	-	$\frac{4}{7}t_{RCIP}$	-	ns
t_{RCIL}	RCLKx_P Low pulse width	-	$\frac{3}{7}t_{RCIP}$	-	ns
t_{RMG}	Receiver Data Input Margin fCLKIN= 60MHz fCLKIN= 65MHz fCLKIN= 66MHz	-0.65	-	0.65	ns
t_{RIP1}	Input Data Position0	$-\lvert t_{RMG}\rvert$	0.0	$+\lvert t_{RMG}\rvert$	ns
t_{RIP0}	Input Data Position1	$\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$\frac{t_{RCIP}}{7}$	$\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns
t_{RIP6}	Input Data Position2	$2\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$2\frac{t_{RCIP}}{7}$	$2\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns
t_{RIP5}	Input Data Position3	$3\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$3\frac{t_{RCIP}}{7}$	$3\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns
t_{RIP4}	Input Data Position4	$4\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$4\frac{t_{RCIP}}{7}$	$4\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns
t_{RIP3}	Input Data Position5	$5\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$5\frac{t_{RCIP}}{7}$	$5\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns
t_{RIP2}	Input Data Position6	$6\frac{t_{RCIP}}{7}-\lvert t_{RMG}\rvert$	$6\frac{t_{RCIP}}{7}$	$6\frac{t_{RCIP}}{7}+\lvert t_{RMG}\rvert$	ns



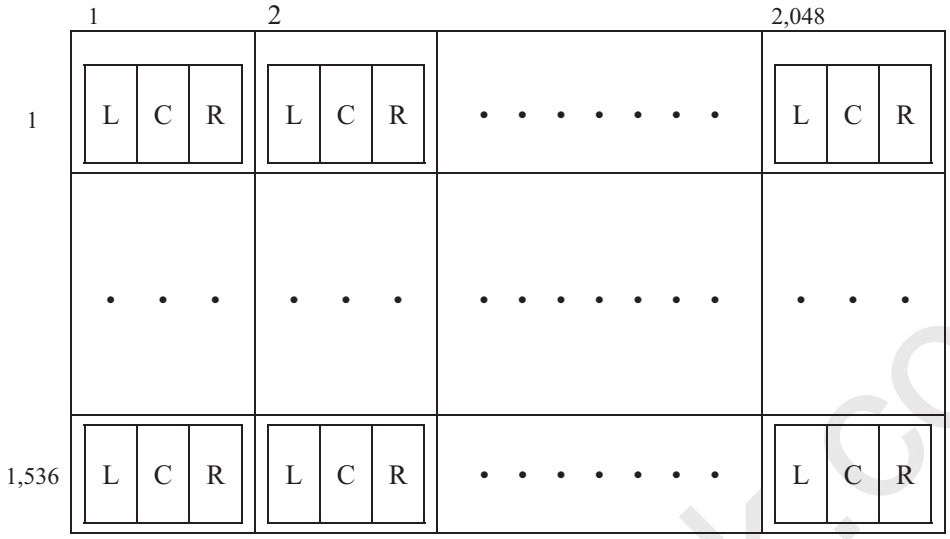
4.12 DISPLAY POSITION

Odd pixel: LA,LC = Left data
CA,CC = Center data
RA,RC = Right data

Even pixel: LB,LD = Left data
CB,CD = Center data
RB,RD = Right data

1, 1	2, 1	• • •	1023, 1	1024, 1	1025, 1	1026, 1	• • •	2047, 1	2048, 1
1, 2	2, 2	• • •	1023, 2	1024, 2	1025, 2	1026, 2	• • •	2047, 2	2048, 2
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1, 1535	2, 1535	• • •	1023, 1535	1024, 1535	1025, 1535	1026, 1535	• • •	2047, 1535	2048, 1535
1, 1536	2, 1536	• • •	1023, 1536	1024, 1536	1025, 1536	1026, 1536	• • •	2047, 1536	2048, 1536

4.13 PIXEL ARRANGNMENT



4.14 OPTICS

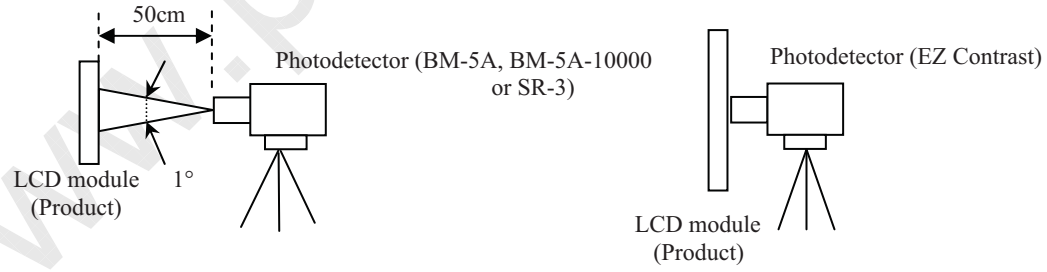
4.14.1 Optical characteristics

(Note1, Note2)

Parameter		Condition	Symbol	min.	typ.	max.	Unit	Measuring instrument	Remarks
Luminance		White at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	L	1,250	1,700	-	cd/m^2	BM-5A or SR-3	Note3
Contrast ratio		White/Black at center θR = 0°, θL = 0°, θU = 0°, θD = 0°	CR	1,000	1,400	-	-	BM-5A or SR-3	Note3 Note5
Luminance uniformity		1023/1023 gray scale θR = 0°, θL = 0°, θU = 0°, θD = 0°	LU$_{1023}$	80	-	-	%	BM-5A or SR-3	Note4 Note6
Chromaticity	White	**x** coordinate	Wx	0.269	0.299	0.329		SR-3	Note3 Note8
		y coordinate	Wy	0.285	0.315	0.345	-		
Color uniformity		818/1023 gray scale θR = 0°, θL = 0°, θU = 0°, θD = 0°	Δu'v'	-	-	0.01	-	SR-3	Note4 Note7
Response time		Black to White	Ton	-	20	30	ms	BM-5A	Note9
		White to Black	Toff	-	20	30	ms		
Viewing angle	Right	θU= 0°、θD= 0°、CR ≥ 10	θR	70	88	-	°	BM-5A or EZ Contrast	Note3 Note10
	Left	θU= 0°、θD= 0°、CR ≥ 10	θL	70	88	-	°		
	Up	θR= 0°、θL= 0°、CR ≥ 10	θU	70	88	-	°		
	Down	θR= 0°、θL= 0°、CR ≥ 10	θD	70	88	-	°		

Note1: These are initial characteristics.
Note2: Measurement conditions are as follows.
Ta= 25°C, VDD= 12.0V, VDDB= 12.0V, PWM: Duty 100%, Display mode: QXGA,
Horizontal cycle= 1/96.72 kHz, Vertical cycle= 1/60.0 Hz

Optical characteristics are measured at luminance saturation 20minutes after the product works in the dark room. Also measurement methods are as follows.



Note3: Product surface temperature at the maximum luminance control: TopF = 29°C
Note4: Product surface temperature at 450cd/m^2 luminance control: TopF = 27°C
Temperature difference in display area: Δ10°C
Note5: See "**4.14.2 Definition of contrast ratio**".
Note6: See "**4.14.3 Definition of luminance uniformity**".
Note7: See "**4.14.4 Definition of color uniformity**".
Note8: These coordinates are found on CIE 1931 chromaticity diagram.
Note9: See "**4.14.5 Definition of response times**".
Note10: See "**4.14.6 Definition of viewing angles**".

4.14.2 Definition of contrast ratio

The contrast ratio is calculated by using the following formula.

$$\text{Contrast ratio (CR)} = \frac{\text{Luminance of white screen}}{\text{Luminance of black screen}}$$

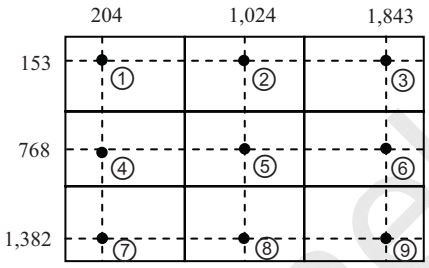
4.14.3 Definition of luminance uniformity

The luminance uniformity is calculated by using following formula.

$$\text{Luminance uniformity (LUxx)} = \frac{\text{Minimum luminance from ① to ⑨}}{\text{Maximum luminance from ① to ⑨}}$$

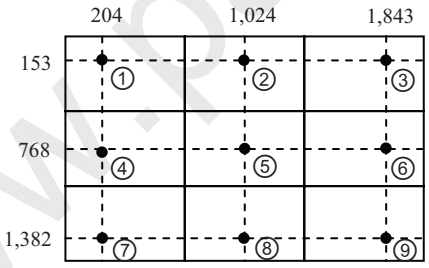
xx: 1023 gray scale.

The luminance is measured at near the 9 points shown below.



4.14.4 Definition of color uniformity

The color (u', v') is measured at near the 9 points shown below



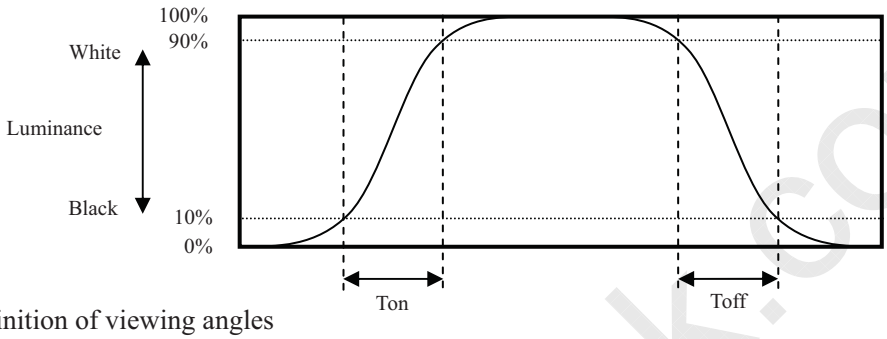
The color uniformity in each measuring point is calculated by using the following formula.

$$\text{Color uniformity}(\Delta u'v') = \sqrt{(u'_x - u'_y)^2 + (v'_x - v'_y)^2}$$

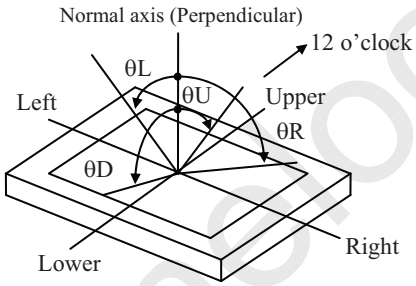
u'_x, v'_x: u', v' value at measuring point x.
u'_y, v'_y: u', v' value at measuring point y.

4.14.5 Definition of response times

Response time is measured at the time when the luminance changes from "black" to "white", or "white" to "black" on the same screen point, by photo-detector. Ton is the time when the luminance changes from 10% up to 90%. Also Toff is the time when the luminance changes from 90% down to 10% (See the following diagram.).
Product surface temperature at the maximum luminance control: TopF= 35°C



4.14.6 Definition of viewing angles

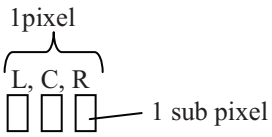


4.15 DEFECT CRITERIA

4.15.1 Display specifications

(Note1)

Defect pattern	Condition			Criteria	Remarks
Line defect	-			0 line	-
Bright dots	Full bright dots Note2			1 dot	-
	Half bright dots Note3	Single defect dot		≤15dots	-
		Linked defect dots (D = 0 mm) Note5	2 defect dots	≤1set	Note6
			3 defect dots or more	0 set	Note7
Dark dots Note4	Single defect dot			≤15dots	-
	Linked defect dots (D = 0 mm) Note5		2 defect dots	≤8set	Note6
			3 -5 defect dots	≤1set	Note7
Close defect dots	Close 2 same color bright dot		Distance between each bright dots ≤6.5mm	L, C, R ≤4 sets each	Note8
Total	Bright dots + Dark dots			≤20dots	-



Note1: Inspection conditions are as follows.

Temperature	25 ± 5 °C
Inspection viewing distance	20 cm (The distance between the inspector's eye and screen.)
Inspection direction	0° ≤ θR ≤ 20°, 0° ≤ θL ≤ 20°
	0° ≤ θU ≤ 20°
Inspection illumination	60 lx (at a display surface)
Luminance	400cd/m^2

Note2: Definition of full bright dot
The full bright dot can be recognized at 160/255 gray scale in full screen in spite of bright dot size.

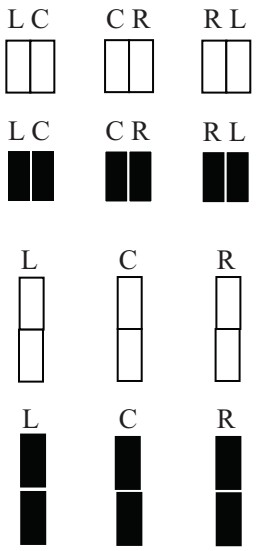
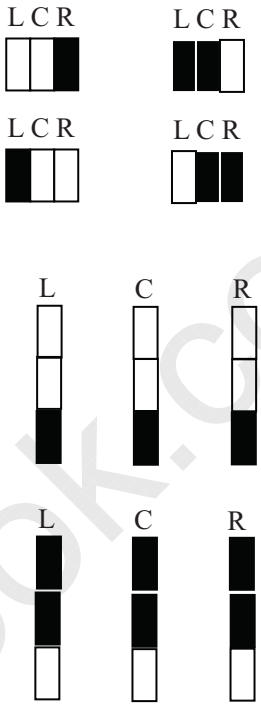
Note3: Definition of half bright dot
The half bright dot can be recognized at 60/255 gray scale in full screen and the defect area is larger than 1/3 of a sub-pixel.

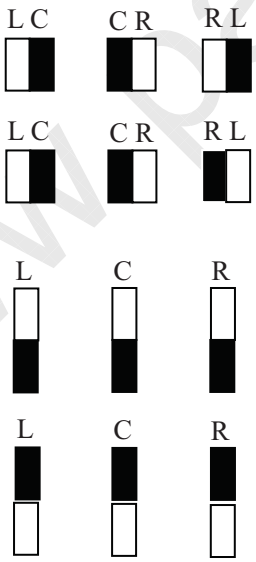
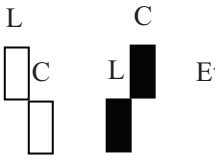
Note4: Definition of dark dot
The dark dot can be recognized at 400cd/m^2 and the defect area is larger than 1/3 of a sub-pixel.

Note5: **D** is the distance between defect dots.

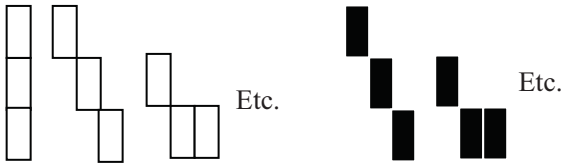
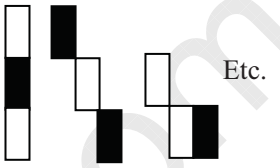
PRELIMINARY

Note6: Linked 2 dots

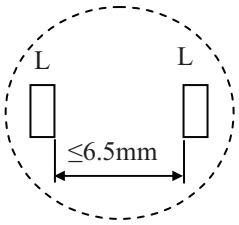
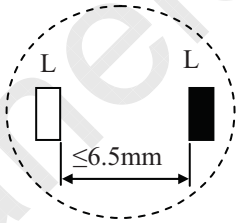
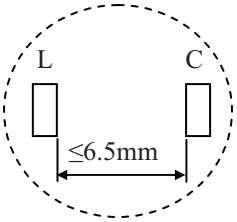
Counted as NG	
	The following combinations are also counted. 

Not counted	
Combinations of bright and dark dots 	Combinations other than linked 2 defect dots 

Note7: Linked 3-5 dots

Counted as NG	Not counted
All of dots are bright dots and dark dots (The Defect criteria for linked 4 or 5 dots are under discussion.) 	Combinations of bright and dark dots 

Note8: Close 2 same color bright dots

Counted as NG	Not counted	
	Combinations of bright and dark dots 	Combinations of different color dots 

4.15.2 Appearance specifications

Defect pattern		Condition Note1		Criteria
Impure ingredient Stains Dust	Dot shape	d < 0.2mm		Allowed
		0.2 mm ≤ d < 0.3 mm		≤ 10 points
		0.3 mm ≤ d ≤ 0.5 mm		≤ 3 points
		d > 0.5mm		0 point
		Linked impure ingredient		
	Line shape	W < 0.05 mm		Allowed
		0.05 mm ≤ W ≤ 0.1 mm	L < 0.7 mm	
			0.7 mm ≤ L ≤ 1.0 mm	≤ 4 points
			L > 1.0 mm	0 point
		W > 0.1 mm		
Bubbles, Wrinkles, Dent		d ≤ 0.2mm		Allowed
		0.2 mm < d ≤ 0.5 mm		≤ 2 points
		d > 0.5mm		0 point
Panel dent		d ≤ 0.2mm		Allowed
		0.2 mm < d ≦ 0.5 mm		≤ 2 points
		d > 0.5mm		0 point
Polarizer scratch		S ≤ 0.2 mm^2		Allowed
		S > 0.2 mm^2		0 point
Shape		Specified label must be put. There must not be a missing part.		

Note1: Definition of symbols is as follows.
d: Average diameter
(This diameter is the average length of a long axis and a short axis in each defect pattern.)
W: Width, L: Length, S: Area

Note2: Inspection conditions are as follows.

Temperature	25 ± 5 °C
Inspection viewing distance	20cm (The distance between the inspector's eye and screen.)
Inspection direction	0° ≤ θR ≤ 45°, 0° ≤ θL ≤ 45°
	0° ≤ θU ≤ 45°, 0° ≤ θD ≤ 45°
Illumination	700 lx (at an inspection desk surface)

5. ESTIMATED LUMINANCE LIFETIME

The luminance lifetime is the time from initial luminance to half-luminance.

This lifetime is the estimated value, and is not guarantee value.

Condition		Estimated luminance lifetime (Life time expectancy) Note1, Note2, Note3	Unit
LED elementary substance	25°C (Ambient temperature of the product) Continuous operation, PWM: Duty 100%	70,000	h
	60°C (Temperature of the product front or rear panel) Continuous operation, PWM: Duty 100%	60,000	

Note1: Life time expectancy is mean time to half-luminance.
Note2: Estimated luminance lifetime is not the value for an LCD module but the value for LED elementary substance.
Note3: By ambient temperature, the lifetime changes particularly. Especially, in case the product works under high temperature environment, the lifetime becomes short.

6. PRODUCT INSPECTIONS

The following inspections are carried out for products, before shipment

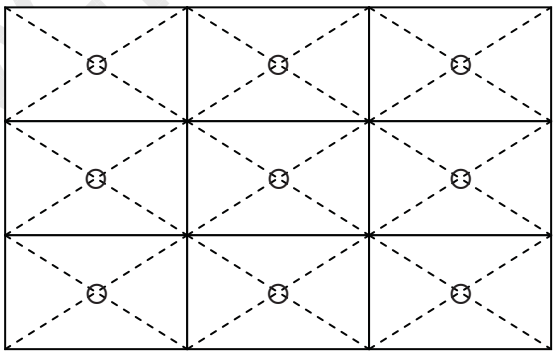
(1) 100% inspection
- Power supply current
- Display
- Appearance

(2) Sampling inspection
- White luminance
- Contrast ratio
- Luminance uniformity

7. RELIABILITY TESTS

Test item		Condition	Judgment Note1
High temperature and humidity (Operation)		① 60 ± 2°C, RH= 60%, 240hours ② Display data is white. Note2	No display malfunctions
Heat cycle (Operation)		① 0 ± 3°C 1hour 60 ± 3°C 1hour ② 50cycles, 4hours/cycle ③ Display data is white. Note2	
Thermal shock (Non operation)		① -20 ± 3°C 30minutes 60 ± 3°C 30minutes ② 100cycles, 1hour/cycle ③ Temperature transition time is within 5 minutes.	
Vibration (Non operation)		① 5 to 100Hz, 11.76m/s^2 ② 1 minute/cycle ③ X, Y, Z directions ④ 10 times each directions	No display malfunctions No physical damages
Mechanical shock (Non operation)		① 294m/s^2, 11ms ② X, Y, Z directions ③ 3 times each directions	
ESD (Operation)		① 150pF, 150Ω, ±10kV ② 9 places on a panel surface Note3 ③ 10 times each places at 1 sec interval	No display malfunctions
Low pressure	Non-operation	① 15 kPa (Equivalent to altitude 13,600m) ② -20°C±3°C 24 hours ③ +60°C±3°C 24 hours	No display malfunctions
	Operation	① 53.3kPa (Equivalent to altitude 5,100m) ② 0°C±3°C 24 hours ③ +60°C±3°C 24 hours Note2	

Note1: Display and appearance are checked under environmental conditions equivalent to the inspection conditions of defect criteria.
Note2: Luminance: 450cd/m^2 at luminance control.
Note3: See the following figure for discharge points



8. MARKINGS

The various markings are attached to this product. See "**11 OUTLINE DRAWINGS**" for attachment positions.

8.1 NAMEPLATE LABEL

Nameplate label

Note1: The meaning of lot number

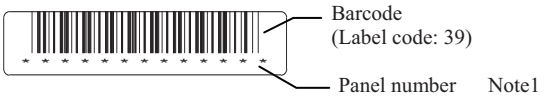
- Example: A3210036

A	3	2	10036
Revision 1 letter (Alphabet)	**Manufacturing year** 1 figure of the A.D. end numbers (e.g.: A.D 2013 is 3.)	**Manufacturing month** 1 letter Jan. to Sep.: Number of month October: A November: B December: C	**Production number** Multi-letter

Note2: **Do not attach anything such as label and so on, on the nameplate!** In case repair the product, NLT needs the contents of nameplate such as the lot number, inspection date and so on, to identify the warranty period with individual product. If NLT cannot decipher the contents of nameplate, such repair shall be entitled to charge. Also NLT may give a new lot number to repair products.

8.2 BARCODE LABEL

Barcode label



Note1: The same panel number is given to barcode label and nameplate label.

8.3 OTHER MARKINGS

Material information marking for diffuser

Material Information
Light Guide >PMMA<

9. PACKING, TRANSPORTATION AND DELIVERY

NLT will pack products to deliver to customer in accordance with NLT's packing specifications, and will deliver products to customer in such a condition that products will not suffer from a damage during transportation. The delivery conditions are as follows.

9.1 PACKING BOX

(1) Inner packing box

5 products are packed as the maximum in an inner packing box (See "**9.5 OUTLINE FIGURE FOR PACKING**"). The type name and quantity are shown on outside of the inner packing box, either labeling or printing. In case the inner packing box with products is dropped from a height of 40cm or more, there is a risk of damage to products.

In case of shipping the product out of Japan, the product must not be transported only with the inner box, because there is a high risk of damage. Be sure to use an outer packing box which is shown below!

(2) Outer packing box

The inner box with products is packed in an outer packing box A or an outer packing box B (See "**9.5 OUTLINE FIGURE FOR PACKING**"). The type name and quantity are shown on outside of the outer packing box, either labeling or printing. In case the outer packing box with products is dropped from a height of 40cm or more, there is a risk of damage to products.

Outer packing box is used only when shipping the product out of Japan.

9.2 INSPECTION RECORD SHEET

Inspection record sheets are included in an inner packing box with products. It is summarized to a number of products for pass/fail assessment.

9.3 TRANSPORTATION

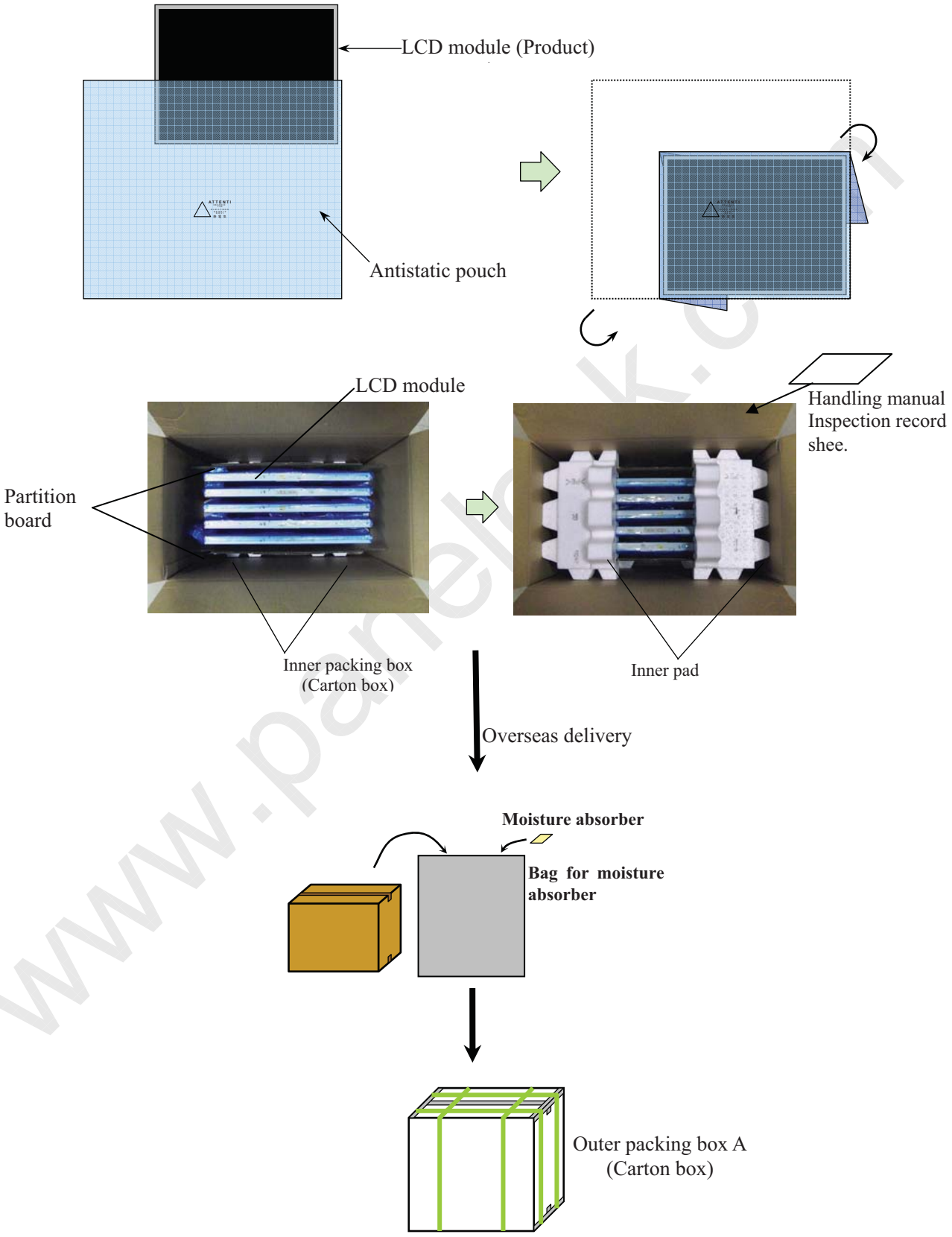
The product is transported by vehicle, aircraft or ship.

9.4 SIZE AND WEIGHT FOR PACKING BOXES

Parameter	Packing box type		Unit
	Inner packing box	Outer packing box	
Size	364(W) × 524(H) × 619(D) (typ.)	397(W) × 576(H) × 647(D) (typ.)	mm
Weight	2.5 (typ.)	1.9 (typ.)	kg
Total weight	16.0 (typ.) (with 5 products)	17.9 (typ.) (with an inner packing box and 5 products)	kg

PRELIMINARY

9.5 OUTLINE FIGURE FOR PACKING



10. PRECAUTIONS

10.1 MEANING OF CAUTION SIGNS

The following caution signs have very important meaning. **Be sure to read "10.2 CAUTIONS" and "10.3 ATTENTIONS"!**

This sign has the meaning that a customer will be injured or the product will sustain damage if the customer practices wrong operations.

This sign has the meaning that a customer will be injured if the customer practices wrong operations.

10.2 CAUTIONS

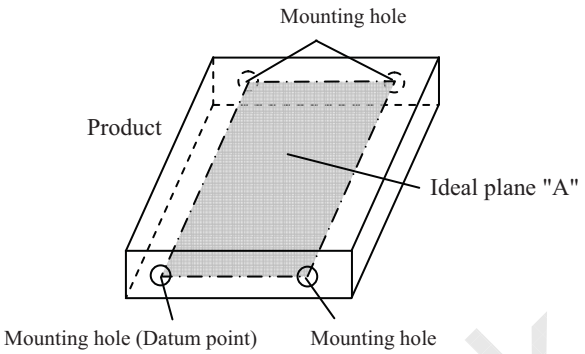
*** Do not shock and press the LCD panel and the backlight! There is a danger of breaking, because they are made of glass. (Shock: Equal to or no greater than 294m/s^2 and equal to or no greater than 11ms, Pressure: Equal to or no greater than 19.6N (ϕ16mm jig))**

10.3 ATTENTIONS

10.3.1 Handling of the product

① Take hold of both ends without touching the circuit board when the product (LCD module) is picked up from inner packing box to avoid broken down or misadjustment, because of stress to mounting parts on the circuit board.
② Do not hook nor pull cables such as lamp cable, and so on, in order to avoid any damage.
③ When the product is put on the table temporarily, display surface must be placed downward.
④ When handling the product, take the measures of electrostatic discharge with such as earth band, ionic shower and so on, because the product may be damaged by electrostatic.
⑤ The torque for product mounting screws must never exceed 0.735N·m. Higher torque might result in distortion of the bezel. And the length of product mounting screws must be ≤ 5.0mm.

⑥ The product must be installed using mounting holes without undue stress such as bends or twist (See outline drawings). And do not add undue stress to any portion (such as bezel flat area). Bends or twist described above and undue stress to any portion may cause display mura.
Recommended installing method: Ideal plane "A" is defined by one mounting hole (datum point) and other mounting holes. The ideal plane "A" should be the same plane within ±0.3 mm.



⑦ Do not press or rub on the sensitive product surface. When cleaning the product surface, wipe it with a soft dry cloth.
⑧ Do not push or pull the interface connectors while the product is working.
⑨ When handling the product, use of an original protection sheet on the product surface (polarizer) is recommended for protection of product surface. Adhesive type protection sheet may change color or characteristics of the polarizer.
⑩ Usually liquid crystals don't leak through the breakage of glasses because of the surface tension of thin layer and the construction of LCD panel. But, if you contact with liquid crystal by any chance, please wash it away with soap and water.

10.3.2 Environment

① Do not operate or store in high temperature, high humidity, dewdrop atmosphere or corrosive gases. Keep the product in packing box with antistatic pouch in room temperature to avoid dusts and sunlight, when storing the product.
② In order to prevent dew condensation occurred by temperature difference, the product packing box must be opened after enough time being left under the environment of an unpacking room. Evaluate the storage time sufficiently because dew condensation is affected by the environmental temperature and humidity. (Recommended leaving time: 6 hours or more with the original packing state after a customer receives the package)
③ Do not operate in high magnetic field. If not, circuit boards may be broken.
④ This product is not designed as radiation hardened.

10.3.3 Characteristics

The following items are neither defects nor failures.

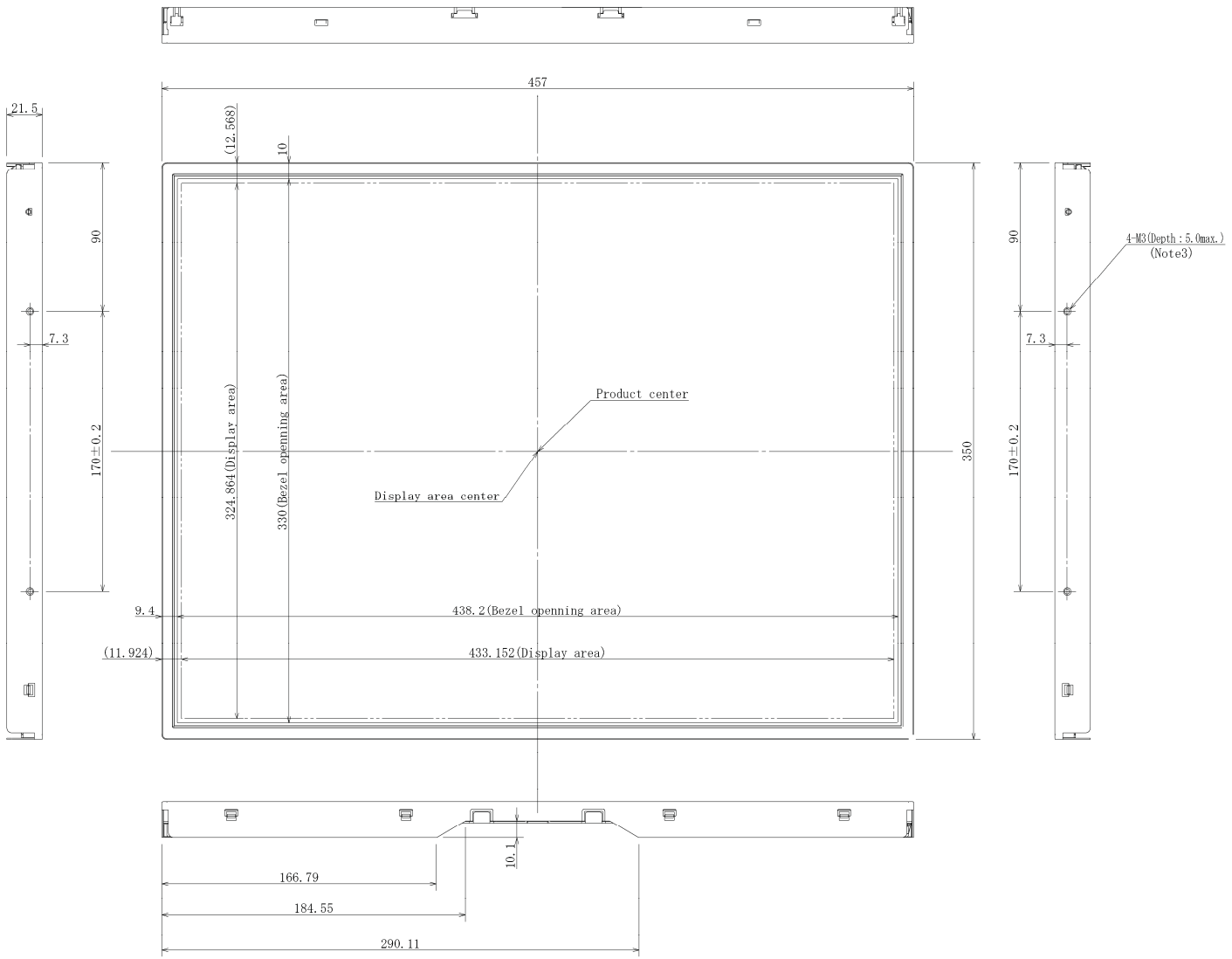
① Response time, luminance and color may be changed by ambient temperature.
② Display mura, flickering, vertical streams or tiny spots may be observed depending on display patterns.
③ Do not display the fixed pattern for a long time because it may cause image sticking. Use a screen saver, if the fixed pattern is displayed on the screen.
④ The display color may be changed depending on viewing angle because of the use of condenser sheet in the backlight.
⑤ Optical characteristics may be changed depending on input signal timings.

10.3.4 Others

① All GND, GNDB, VDD and VDDB terminals should be used without any non-connected lines.
② Do not disassemble a product or adjust variable resistors.
③ Pack the product with the original shipping package, in order to avoid any damages during transportation, when returning the product to NLT for repairing and so on.
④ The LCD module by itself or integrated into end product should be packed and transported with display in the vertical position. Otherwise the display characteristics may be degraded.

11. OUTLINE DRAWINGS

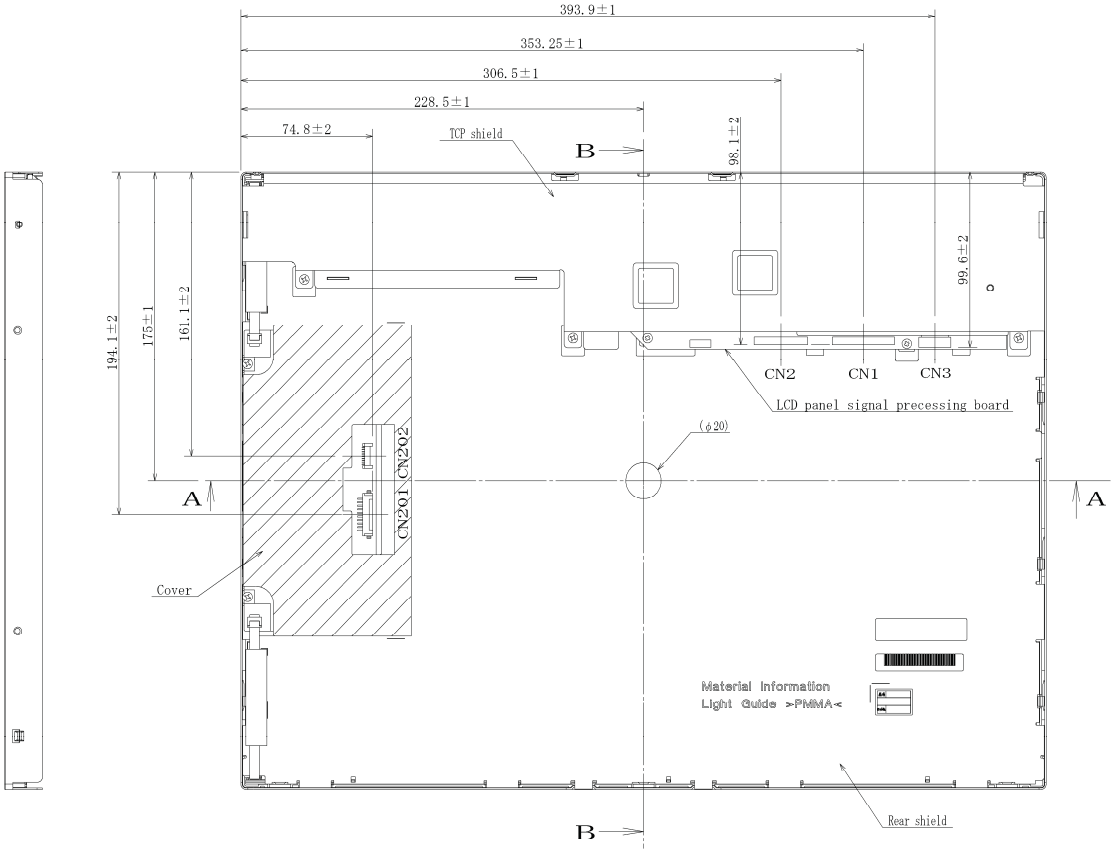
11.1 FRONT VIEW

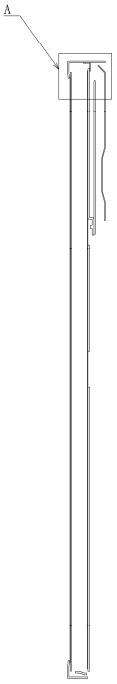


(Unit: mm)

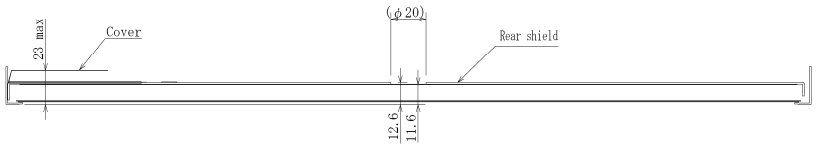
Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The length of product mounting screws from surface of plate must be ≤ 5.0mm.
Note4: The values in parentheses are for reference.

11.2 REAR VIEW

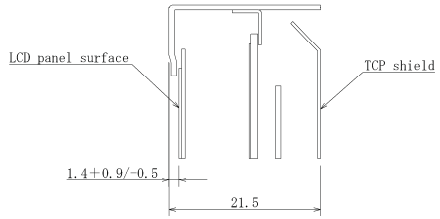




Sec. B–B



Sec. A–A



Detail A

Note1: Not shown tolerances of the dimensions are ±0.5mm.
Note2: The torque for product mounting screws must never exceed 0.735N·m.
Note3: The values in parentheses are for reference.
Note4: The length of product mounting screws from surface of plate must be ≤ 5.0mm.

(Unit: mm)

PRELIMINARY

REVISION HISTORY

The inside of latest specifications is revised to the clerical error and the major improvement of previous edition. Only a changed part such as functions, characteristic value and so on that may affect a design of customers, are described especially below.

Edition	Prepared date	Revision contents and signature	Issued date
1st edition	Feb. 1, 2013	**Revision contents** New issue **Signature of writer** *Approved by* K. Fujimoto — K. FUJIMOTO *Checked by* — *Prepared by* E. Yoshimura — E. YOSHIMURA	